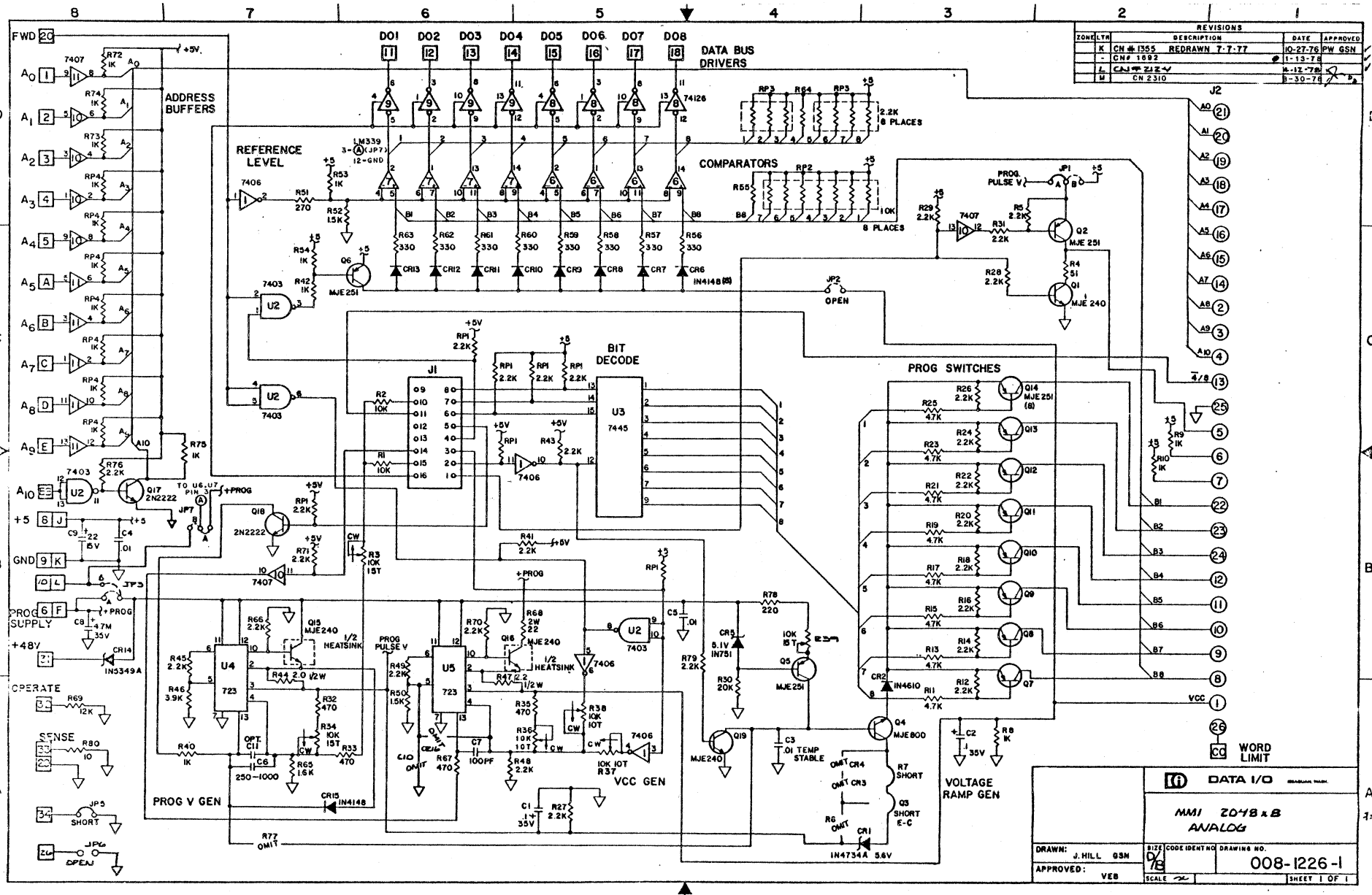
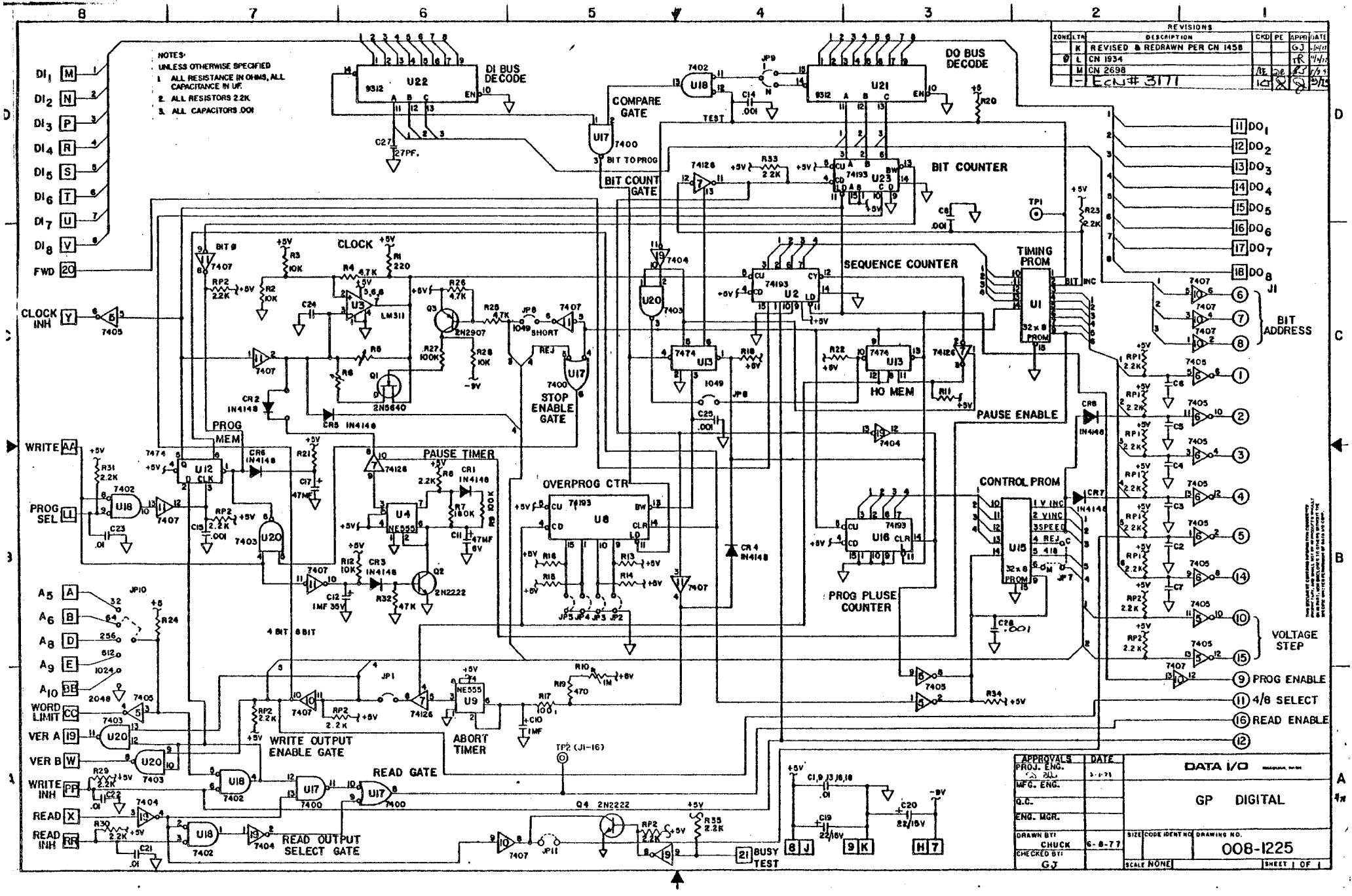
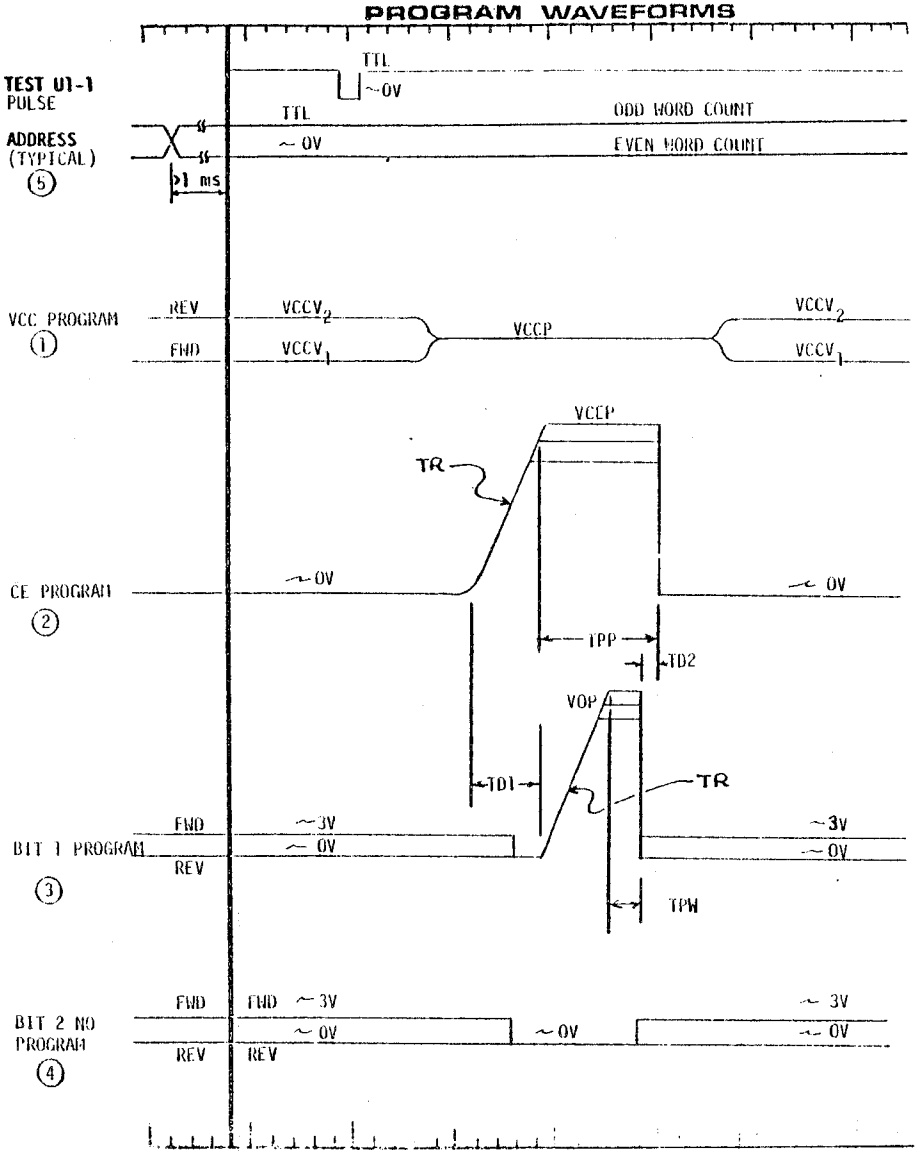

REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
K CN # 1355 REDRAWN 7-7-77 10-27-76 PW GSN
- CN# 1692 1-13-78
L CN # 2172 4-12-78
M CN 2310 8-30-78
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8
DATA BUS DRIVERS
ADDRESS BUFFERS
REFERENCE LEVEL
COMPARATORS
BIT DECODE
PROG SWITCHES
PROG V GEN
VCC GEN
VOLTAGE RAMP GEN
PROG SUPPLY
SENSE
OPERATE
WORD LIMIT
DATA I/O
MMI 2048 x 8
ANALOG
DRAWN: J. HILL GSN
APPROVED: VEB
SIZE D/8
CODE IDENT NO
DRAWING NO. 008-1226-1
SCALE
SHEET 1 OF 1


NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE IN OHMS, ALL CAPACITANCE IN UF.
2. ALL RESISTORS 2.2K
3. ALL CAPACITORS .001
REVISIONS
ZONE | LTR | DESCRIPTION | CKD | PE | APPR | DATE
K REVISED & REDRAWN PER CN 1458 GJ
@ L CN 1934
M CN 2698
- ECN# 3171
DI BUS DECODE
DO BUS DECODE
COMPARE GATE
BIT COUNTER
BIT COUNT GATE
SEQUENCE COUNTER
TIMING PROM
CLOCK
PROG MEM
PAUSE TIMER
STOP ENABLE GATE
PAUSE ENABLE
HO MEM
OVERPROG CTR
PROG PLUSE COUNTER
CONTROL PROM
BIT ADDRESS
VOLTAGE STEP
WRITE OUTPUT ENABLE GATE
READ GATE
ABORT TIMER
READ OUTPUT SELECT GATE
DI1 DI2 DI3 DI4 DI5 DI6 DI7 DI8 FWD
CLOCK INH
WRITE PROG SEL
WORD LIMIT VER A VER B WRITE INH READ READ INH
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8
PROG ENABLE
4/8 SELECT
READ ENABLE
BUSY TEST
APPROVALS DATE
PROJ. ENG.
MFG. ENG.
Q.C.
ENG. MGR.
DRAWN BY! CHUCK 6-8-77
CHECKED BY! GJ
DATA I/O
GP DIGITAL
SIZE CODE IDENT NO DRAWING NO.
008-1225
SCALE NONE SHEET 1 OF 1

779	-	ECR#3067	EP	8-30-78	E	LCN #2310		DB			DATE	SYM	REVISION RECORD	DR	CK
				9-15-78	-	LCN #2756		RC			4-76	B	CN #610	LC	TI
				11-28-78	-	ECR #3694		FS			-76	C	CN #761	KJ	TS
											3-77	D	CN #1125	DR	JEB
											9-1-77	-	CORRECTED Vcc PROG. NUM.	DR	DR

PROGRAM WAVEFORMS



NOTES

For calibration, the card set polarity defaults to VOL.

DIGITAL CARD JUMPERS - 1225

- JP1 = OPEN
- JP2 = SHORT
- JP3 = SHORT
- JP4 = SHORT
- JP5 = SHORT
- JP6 = OPEN
- JP7C = 9 PULSE REJECT
- JP7M = 1 PULSE REJECT
- JP8 = OPEN
- JP9 = N
- JP10 = WORD LIMIT = 2048
- JP11 = SHORT

ABORT TIMER = JP1 - NOT USED

PAUSE TIMER (CR2) = NOT USED

WAVEFORM VARIABLES

- TPP = 30 μSEC ≤ TPP ≤ 100 μSEC
- TR = .4V/μSEC ±15%
- TD1 ≥ 10 μSEC
- TD2 ≥ 100 n sec
- TPW = 7 ± 5 u sec
- $VCCV_1$ = 4.2 ± .25 V
- $VCCV_2$ = 6.0 ± .25 V
- VCCP = 5.5 + 0.25 V

NOTE: TR ADJUST FOR BIT 1 PROGRAM = ANALOG R39

PULSE NO.	VCEP*	VOP*
1 - 3	27	20
4 - 6	30	23
7 - 9	33	26

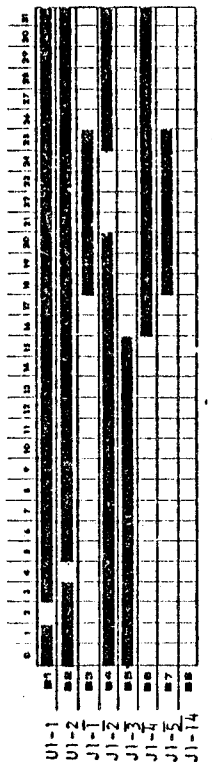
* ± 1.0V Tolerance

These waveforms correspond to callouts on the Calibration Chart. Switch S2 and S3 of the Universal Calibrator to indicated positions to obtain waveforms. Refer to Performance Check section of manual for detailed steps.

TRUTH TABLES

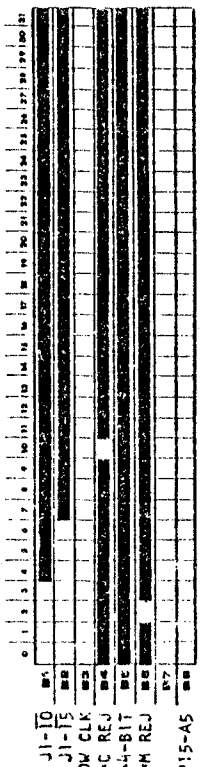
LINE : HI(1); NO LINE : LOW(Ø)

TIMING ROM U1



TIMING PROM COUNT

MODE ROM U15



DATA I/O

TITLE	TIMING DIAGRAM
DRAWN	K. JONES
	M.M.I. GENERIC
DATE	12-1-75
DRAWING NO.	007-1226-1

3/78

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

CALIBRATION CHART 017-1226-1 | PROGRAM CARD 909-1226-1
FIXTURE 702-1071 | MANUFACTURER MONOLITHIC MEMORIES
PROGRAM ADAPTER 910-1226-1 | PROM M. M. I. GENERIC FAMILY

DATE	REV	REVISION RECORD	DR	CK
2-77	E	C.N. #1053	KJ	DP
4-16-77	-	C.N. #1238	PW	DP
7-9-77	F	C.N. #1520 (re-typed)	GJ	
10-19-77	-	P9 update,CN #1996	GJ	GJ
11-77	-	E.C.N. #2565	FS	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
7F	E8	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5	Adjustments are located on the power supply board.
7F	E8	FIXED +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8	
7F	E8	SUPPLIES +5	1-3	000	00	000			+5	R18	5.05	5.1	5.15	See programmer manual.
7F	E8	-9	1-4	000	00	000			-9	R40	-8.8	-9.0	-9.2	See NOTE 1.
7F	E8	PROGRAMMABLE SUPPLY	1-5	000	00	000	7	1	PROG V.		28.0		36.0	
7F	E8	VCC VERIFY LOW, V SET	2-1	001	01	001	5	1	TP3	R36	3.95	4.2	4.45	Set programmer in FWD. *Adjustment Step.*
7F	E8	VCC VERIFY HIGH, V SET	2-2	000	00	000	5	1	TP3	R38	5.75	6.0	6.25	Set programmer in REV. *Adjustment Step.*
7F	EC	VCC PROGRAM, V SET (1)	2-3	002	02	002	5	1	TP3	R37	5.25	5.5	5.75	*Adjustment Step.*
7F	EC	VCC CURRENT, ICC LIMIT	2-4	003	03	003	6	1	TP3		2.0		3.0	See NOTE 2.
7F	EC	VERIFY LOGIC LOW LEVEL	3-1	004	04	004	7	8	U6 P8		0.9		1.1	Set programmer in FWD. Test point located on analog card.
7F	EC	VERIFY LOGIC HIGH LEVEL	3-2	003	03	003	7	8	U6 P8		2.8		3.2	Set programmer in REV. Test point located on analog card.
7F	EC	BIT 8 VOL LOAD VERIFY	3-3	004	04	004	2	8	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 8 VOH LOAD VERIFY	3-4	003	03	003	2	8	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 7 VOL LOAD VERIFY	3-5	004	04	004	2	9	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 7 VOH LOAD VERIFY	3-6	003	03	003	2	9	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 6 VOL LOAD VERIFY	3-7	004	04	004	2	10	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 6 VOH LOAD VERIFY	3-8	003	03	003	2	10	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 5 VOL LOAD VERIFY	3-9	004	04	004	2	11	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 5 VOH LOAD VERIFY	3-10	003	03	003	2	11	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 4 VOL LOAD VERIFY	3-11	004	04	004	2	12	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 4 VOH LOAD VERIFY	3-12	003	03	003	2	12	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 3 VOL LOAD VERIFY	3-13	004	04	004	2	23	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 3 VOH LOAD VERIFY	3-14	003	03	003	2	23	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 2 VOL LOAD VERIFY	3-15	004	04	004	2	22	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 2 VOH LOAD VERIFY	3-16	003	03	003	2	22	TP3		2.1		2.9	Set programmer in REV.
7F	EC	BIT 1 VOL LOAD VERIFY	3-17	004	04	004	2	21	TP3		3.8		4.8	Set programmer in FWD.
7F	EC	BIT 1 VOH LOAD VERIFY	3-18	003	03	003	2	21	TP3		2.1		2.9	Set programmer in REV.
7F	EC	$\overline{E2}$ PROGRAM, VPP LOW SET (2)	4-1	005	05	005	4	5	TP3	R34	26.0	27.0	28.0	*Adjustment Step.*
3D	EC	$\overline{E2}$ PROGRAM, VPP HIGH SET	4-2	006	06	006	4	5	TP3	R3	32.0	33.0	34.0	*Adjustment Step.*

COMMENTS
NOTES are on page 3.
Switch S1 must be depressed for accurate readings.
CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	
7D	EC	$\overline{E2}$ PROGRAM, VPP MEDIUM	4-3	007	07	007	4	5	TP3		29.0		31.0	
7D	EC	$\overline{E2}$ CURRENT, IPP LIMIT	4-4	007	07	007	6	5	TP3		2.5		3.5	CAUTION! See NOTE 2.
3D	ED	$\overline{E2}$ VERIFY	4-5	008	08	010	10	5	TP3		0.0		0.4	
3D	ED	E3 & E4 PROGRAM/VERIFY	4-6	008	08	010	7	6 & 7	TP3		5.0		5.15	2 Tests. See NOTE 1.
BD	E6	BIT 8 PROGRAM	5-1	009	09	011	3	8	TP3		25.0		27.0	
BD	E6	BIT CURRENT LIMIT	5-2	009	09	011	6	8	TP3		2.5		3.5	
BD	C6	BIT 8 DESELECT	5-3	010	0A	012	3	8	TP3		0.0		0.9	Confirm bit 8 ON (HEX 7F) on DO Bus.
BD	C6	BIT 7 PROGRAM	5-4	011	0B	013	3	9	TP3		25.0		27.0	
BD	A6	BIT 7 DESELECT	5-5	012	0C	014	3	9	TP3		0.0		0.9	Confirm bit 7 ON (HEX BF) on DO Bus.
BD	A6	BIT 6 PROGRAM	5-6	013	0D	015	3	10	TP3		25.0		27.0	
BD	86	BIT 6 DESELECT	5-7	014	0E	016	3	10	TP3		0.0		0.9	Confirm bit 6 ON (HEX DF) on DO Bus.
BD	86	BIT 5 PROGRAM	5-8	015	0F	017	3	11	TP3		25.0		27.0	
BD	66	BIT 5 DESELECT	5-9	016	10	020	3	11	TP3		0.0		0.9	Confirm bit 5 ON (HEX EF) on DO Bus.
BD	66	BIT 4 PROGRAM	5-10	017	11	021	3	12	TP3		25.0		27.0	
BD	46	BIT 4 DESELECT	5-11	018	12	022	3	12	TP3		0.0		0.9	Confirm bit 4 ON (HEX F7) on DO Bus.
BD	46	BIT 3 PROGRAM	5-12	019	13	023	3	23	TP3		25.0		27.0	
BD	26	BIT 3 DESELECT	5-13	020	14	024	3	23	TP3		0.0		0.9	Confirm bit 3 ON (HEX FB) on DO Bus.
BD	26	BIT 2 PROGRAM	5-14	021	15	025	3	22	TP3		25.0		27.0	
BD	06	BIT 2 DESELECT (4)	5-15	022	16	026	3	22	TP3		0.0		0.9	Confirm bit 2 ON (HEX FD) on DO Bus.
BD	06	BIT 1 PROGRAM (3)	5-16	023	17	027	3	21	TP3		25.0		27.0	
BD	26	BIT 1 DESELECT	5-17	024	18	030	3	21	TP3		0.0		0.9	Confirm bit 1 ON (HEX FE) on DO Bus.
3D	3C	PROGRAM V. KILL	5-18	025	19	031	4	5	TP3		0.0		0.4	
BD	C6	ADDRESS TEST VIL, A0 (5)	6-1	682	2AA	1252	7	20	TP3		0.0		0.4	
BD	C6	ADDRESS TEST VIH, A1	6-2	682	2AA	1252	7	19	TP3		4.8		5.15	
BD	C6	ADDRESS TEST VIL, A2	6-3	682	2AA	1252	7	18	TP3		0.0		0.4	
BD	C6	ADDRESS TEST VIH, A3	6-4	682	2AA	1252	7	17	TP3		4.8		5.15	
BD	C6	ADDRESS TEST VIL, A4	6-5	682	2AA	1252	7	16	TP3		0.0		0.4	
BD	C6	ADDRESS TEST VIH, A5	6-6	682	2AA	1252	7	15	TP3		4.8		5.15	
BD	C6	ADDRESS TEST VIL, A6	6-7	682	2AA	1252	7	14	TP3		0.0		0.4	
BD	C6	ADDRESS TEST VIH, A7	6-8	682	2AA	1252	7	13	TP3		4.8		5.15	
BD	C6	ADDRESS TEST VIL, A8	6-9	682	2AA	1252	7	2	TP3		0.0		0.4	

CALIBRATION CHART 017-1226-1

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
BD	C6	ADDRESS TEST VIH, A9	6-10	682	2AA	1252	7	3	TP3		4.8		5.15
BD	C6	ADDRESS TEST VIL, A10	6-11	682	2AA	1252	7	4	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A0	6-12	1365	555	2525	7	20	TP3		4.8		5.15
BD	26	ADDRESS TEST VIL, A1	6-13	1365	555	2525	7	19	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A2	6-14	1365	555	2525	7	18	TP3		4.8		5.15
BD	26	ADDRESS TEST VIL, A3	6-15	1365	555	2525	7	17	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A4	6-16	1365	555	2525	7	16	TP3		4.8		5.15
BD	26	ADDRESS TEST VIL, A5	6-17	1365	555	2525	7	15	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A6	6-18	1365	555	2525	7	14	TP3		4.8		5.15
BD	26	ADDRESS TEST VIL, A7	6-19	1365	555	2525	7	13	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A8	6-20	1365	555	2525	7	2	TP3		4.8		5.15
BD	26	ADDRESS TEST VIL, A9	7-1	1365	555	2525	7	3	TP3		0.0		0.4
BD	26	ADDRESS TEST VIH, A10	7-2	1365	555	2525	7	4	TP3		4.8		5.15
BD	26	GROUND TEST	7-3	1365	555	2525	8	24	TP3		0.0		0.08
7F	AD	←—DATA PATTERN FOR ALL WORDS NOT SHOWN											

NOTES:

1. For the System 19, the limits for this test are .01 volt less than specified.
2. Do not hold S1 depressed for extended periods.